Refine Search

Search Results -

Terms	Documents
(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy$3) same (FIFO or buffer)	37

Database:
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Search History

DATE: Wednesday, August 18, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L1	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy$3) same (FIFO or buffer)	37	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(707/201 |370/401 |370/402 |709/213 |709/214 |709/253 |710/306 |710/312 |710/112 |711/141 |711/148).ccls.	4925

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
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- EPO Abstracts Database
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- IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, August 18, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L1	710/306,312,112;711/141,148;709/213,214,253;370/401-402;707/201.ccls.	4925	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L1 and L2	45

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

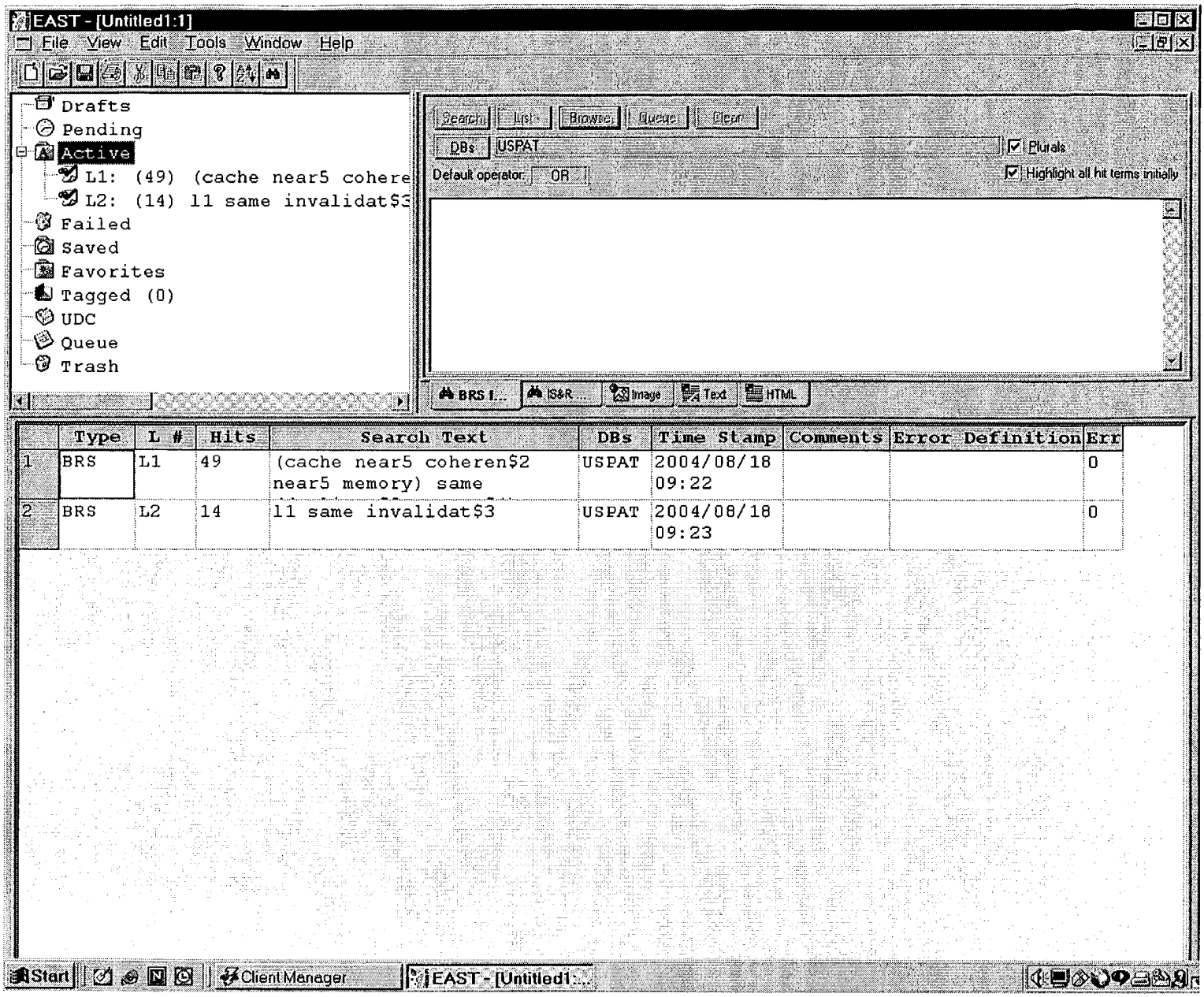
Recall Text Clear Interrupt

Search History

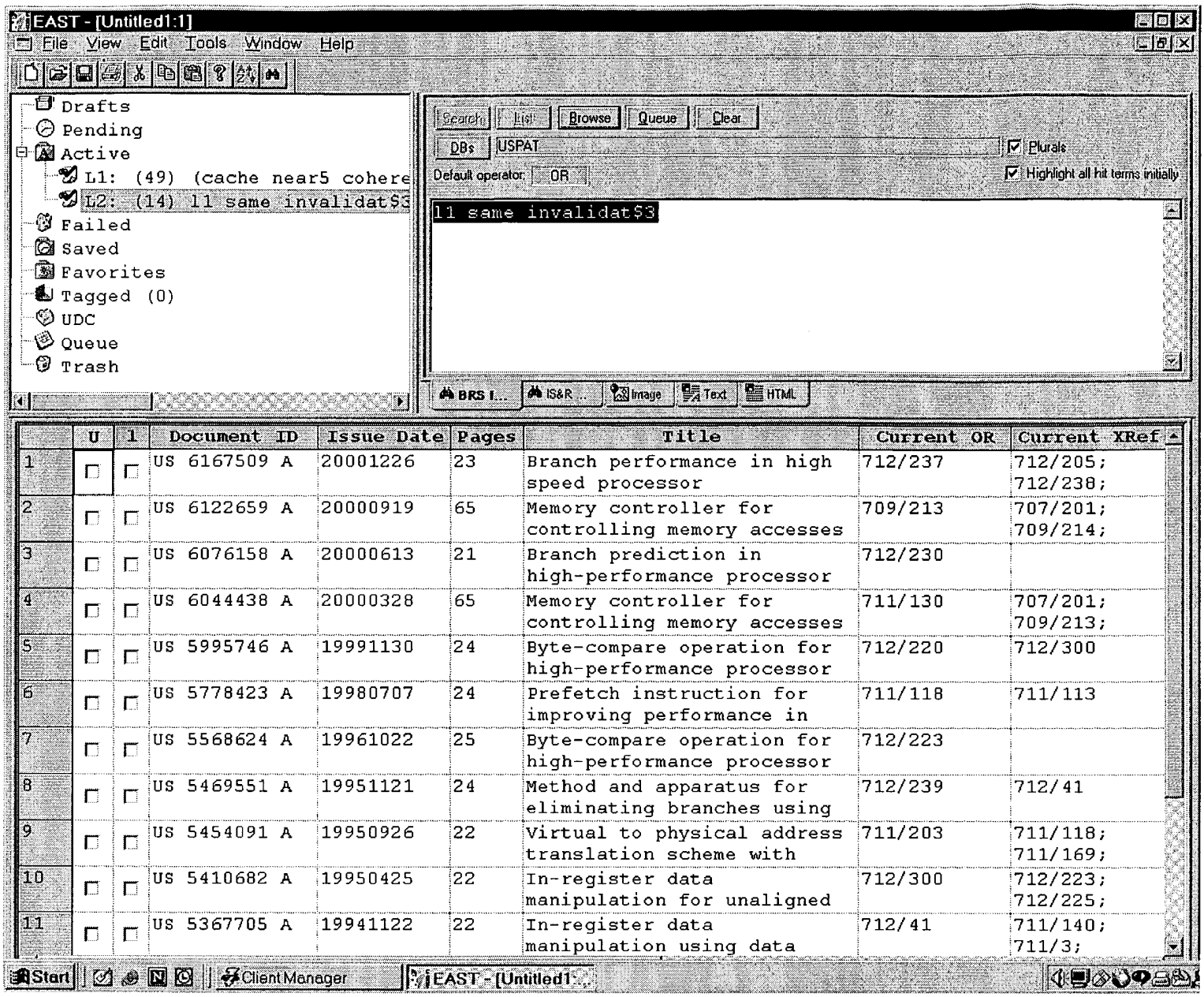
DATE: Wednesday, August 18, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	l1 and L2	45	L3
L2	cache same coheren$2 same memory same (duplicat$3 or cop$4) same (FIFO or buffer)	127	L2
L1	710/306,312,112;711/141,148;709/213,214,253;370/401-402;707/201.ccls.	4925	L1

END OF SEARCH HISTORY



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	49	(cache near5 coheren$2 near5 memory) same	USPAT	2004/08/18 09:22			0
2	BRS	L2	14	l1 same invalidat$3	USPAT	2004/08/18 09:23			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6167509 A	20001226	23	Branch performance in high speed processor	712/237	712/205; 712/238;
2	☐	☐	US 6122659 A	20000919	65	Memory controller for controlling memory accesses	709/213	707/201; 709/214;
3	☐	☐	US 6076158 A	20000613	21	Branch prediction in high-performance processor	712/230	
4	☐	☐	US 6044438 A	20000328	65	Memory controller for controlling memory accesses	711/130	707/201; 709/213;
5	☐	☐	US 5995746 A	19991130	24	Byte-compare operation for high-performance processor	712/220	712/300
6	☐	☐	US 5778423 A	19980707	24	Prefetch instruction for improving performance in	711/118	711/113
7	☐	☐	US 5568624 A	19961022	25	Byte-compare operation for high-performance processor	712/223	
8	☐	☐	US 5469551 A	19951121	24	Method and apparatus for eliminating branches using	712/239	712/41
9	☐	☐	US 5454091 A	19950926	22	Virtual to physical address translation scheme with	711/203	711/118; 711/169;
10	☐	☐	US 5410682 A	19950425	22	In-register data manipulation for unaligned	712/300	712/223; 712/225;
11	☐	☐	US 5367705 A	19941122	22	In-register data manipulation using data	712/41	711/140; 711/3;

Your search matched **1** of **1062489** documents.
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cache and coheren*<and>(fifo or buffer) and invalid* Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Photonic architectures for distributed shared memory multiprocess**
Dowd, P.W.; Chu, J.;
Massively Parallel Processing Using Optical Interconnections, 1994., Proceedi the First International Workshop on , 26-27 April 1994
Pages:151 - 161

[Abstract] [PDF Full-Text (904 KB)] **IEEE CNF**

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Photonic architectures for distributed shared memory multiprocessors

Dowd, P.W. Chu, J.
Dept. of Electr. & Comput. Eng., State Univ. of New York, Buffalo, NY, USA;

This paper appears in: **Massively Parallel Processing Using Optical Interconnections, 1994., Proceedings of the First International Workshop on**

Meeting Date: 04/26/1994 - 04/27/1994
Publication Date: 26-27 April 1994
Location: Cancun Mexico
On page(s): 151 - 161
Reference Cited: 20
Inspec Accession Number: 4677984

Abstract:
This paper studies the interaction between the access protocol used to provide arbitration for a wavelength-division multiple access photonic network and the **cache coherence** protocol required to support a distributed shared memory environment. The architecture is based on wavelength division multiplexing which enables multiple multi-access channels to be realized on a single optical fiber. Larger blocks are supported to reduce the per bit overhead and increase the exploitation of spatial locality, while false sharing is reduced through a mechanism to provide a finer granularity of **invalidation**. Two main

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Print Format

approaches have been considered to harness the enormous **available** bandwidth of WDMA optical networks: reservation (control-channel based) or pre-allocation media access protocols. This paper extends the function of a control channel to include broadcast support of **cache**-level control information, in addition to its primary role of data channel reservation, thereby enabling a snooping based **coherence** protocol to be considered. Larger snooping-based multiprocessors may be possible with this approach. Two major scenarios are considered through trace-based discrete-event simulation in this paper: a system with a directory based **cache coherence** protocol and a pre-allocation based WDMA access protocol is compared to a system with a snooping based **cache coherence** protocol and a reservation based WDMA access protocol

Index Terms:

buffer storage distributed memory systems optical information processing optical links parallel architectures shared memory systems wavelength division multiplexing WDMA optical networks access protocol **cache coherence** protocol **cache**-level control information control channel distributed shared memory multiprocessors false sharing optical fiber photonic architectures pre-allocation media access protocols reservation snooping based **coherence** protocol snooping-based multiprocessors spatial locality trace-based discrete-event simulation wavelength division multiplexing wavelength-division multiple access photonic network

Documents that cite this document

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L3: Entry 9 of 45 File: USPT Sep 16, 2003

US-PAT-NO: 6622214
DOCUMENT-IDENTIFIER: US 6622214 B1

TITLE: System and method for maintaining memory coherency in a computer system having multiple system buses

DATE-ISSUED: September 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Vogt; Pete D.	Boulder	CO		
White; George P.	Long Beach	CA		
Chang; Stephen S.	Glendora	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 228665 [PALM]
DATE FILED: January 12, 1999

PARENT-CASE:
This U.S. Patent application is a divisional application of U.S. patent application Ser. No. 08/714,750, filed Sep. 16, 1996, now U.S. Pat. No. 5,897,656.

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 711/141; 711/124, 711/146
US-CL-CURRENT: 711/141; 711/124, 711/146

FIELD-OF-SEARCH: 711/141, 711/143-145, 711/133, 711/159, 711/146, 711/124, 711/154, 711/130, 711/210, 710/100, 710/107, 710/128, 710/54-55, 710/305, 710/309-310

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4245344	January 1981	Richter	714/43
☐	4796232	January 1989	House	365/189.03
☐	4953081	August 1990	Feal et al.	710/111

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☐	4982321	January 1991	Pantry et al.	710/107
☐	5115411	May 1992	Kass et al.	365/189.01
☐	5119485	June 1992	Ledbetter, Jr. et al.	711/146
☐	5193163	March 1993	Sanders et al.	711/122
☐	5225374	July 1993	Fare et al.	438/1
☐	5265211	November 1993	Amini et al.	710/36
☐	5269005	December 1993	Heil et al.	710/49
☐	5293603	March 1994	MacWilliams et al.	710/129
☐	5319766	June 1994	Thaller et al.	711/146
☐	5325510	June 1994	Frazier	711/118
☐	5359715	October 1994	Heil et al.	710/128
☐	5369748	November 1994	McFarland et al.	710/126
☐	5369753	November 1994	Tipley	711/122
☐	5386517	January 1995	Sheth et al.	710/60
☐	5398325	March 1995	Chang et al.	711/3
☐	5404462	April 1995	Datwyler et al.	713/600
☐	5414820	May 1995	McFarland et al.	710/128
☐	5442754	August 1995	Datwyler et al.	710/128
☐	5495570	February 1996	Heugel et al.	714/11
☐	5495585	February 1996	Datwyler et al.	710/100
☐	5553258	September 1996	Godiwala et al.	711/3
☐	5553263	September 1996	Kalish et al.	711/127
☐	5644753	July 1997	Ebrahim et al.	711/131
☐	5673400	September 1997	Kenny	710/129
☐	5684977	November 1997	Van Loo et al.	711/143
☐	5740400	April 1998	Bowles	711/144
☐	5822755	October 1998	Shippy	711/118
☐	5828835	October 1998	Isfeld et al.	709/200
☐	5829033	October 1998	Hagersten et al.	711/141
☐	5857084	January 1999	Klein	710/129
☐	5900011	May 1999	Saulsbury et al.	711/119

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
195 06 734	September 1995	DE	
0 507 063	October 1992	EP	

OTHER PUBLICATIONS

h e b b g e e e f c e f e ge

Corollary Inc., Gemini External Design Specification, Dec. 4, 1995, pp. 1-107.*
"VIC 8251F VIC to VME Interface with Mirrored Memory," Creative Electronic Systems, Version 1.1, Jun. 1994, pp. 1-103, XP002198526, Petit-Lancy, Switzerland.
"IBM patents--Abstract/Exempt Claim", U.S. patent No. 5,018,053 issued May 21, 1991, patent title "Method for Reducing Cross-Interrogate Delays in a Multiprocessor System", Micron Technology Confidential Information, p. 2658, Mar. 27, 1996.
Customer Request Summary--E014 Full-Text Patent Report, U.S. Patent No. 5,369,753, issued Nov. 29, 1994, patent title "Method and Apparatus for Achieving Multilevel Inclusion in Multilevel Cache Hierarchies", SPO Services Results, 18 pages, Mar. 13, 1996.
Anderson, Don, et al., "Chapter 4: Multiple Processors and the MESI Model", Pentium.TM. Processor System Architecture, pp. 65-91, 1995.
Glaskowsky, Peter N., "Profusion Adds Processors and Performance: Corollary Creates Credible Chip Set for 8-CPU Pentium Pro Servers", Microdesign Resources, 2 pages, Sep. 16, 1996.
"ULTRASPARC.TM.--Ultra Port Architecture (UPA): The New-Media System Architecture", from Sun Microelectronics, 4 pages, last updated Jun. 6, 1996.
"Gemini External Design Specification", Corollary Confidential Document, pp. i-107, Dec. 4, 1995.
"Gemini Reference Platform Specification", Corollary Confidential Document, pp. i-29, Mar. 15, 1996.
Handy, Jim, "Chapter 4: Maintaining Coherency in Cached Systems", The Cache Memory Book, pp. 125-190, 1993.

ART-UNIT: 2186

PRIMARY-EXAMINER: Kim; Matthew

ASSISTANT-EXAMINER: Tran; Denise

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

A cache-coherent, multiple-bus, multiprocessing system and method interconnects multiple system buses and an I/O bus to a shared main memory and efficiently maintains cache coherency while minimizing the impact to latency and total bandwidth within the system. The system provides coherency filters which coordinate bus-to-bus communications in such a way as to maintain cache memory coherency with a small amount of cross-bus traffic. In addition, the system provides a multiported pool of memory cells which interconnect the multiple buses.

9 Claims, 11 Drawing figures

Previous Doc Next Doc Go to Doc#

L3: Entry 36 of 45 File: USPT Mar 30, 1999

US-PAT-NO: 5890217
DOCUMENT-IDENTIFIER: US 5890217 A

TITLE: Coherence apparatus for cache of multiprocessor

DATE-ISSUED: March 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kabemoto; Akira	Kawasaki			JP
Shibata; Naohiro	Kawasaki			JP
Muta; Toshiyuki	Kawasaki			JP
Shimamura; Takayuki	Kawasaki			JP
Sugahara; Hirohide	Kawasaki			JP
Nishioka; Junji	Kawasaki			JP
Sasaki; Takatsugu	Kawasaki			JP
Shinohara; Satoshi	Kawasaki			JP
Nakayama; Yozo	Aza Unoke-machi			JP
Sakurai; Jun	Sendai			JP
Ishihata; Hiroaki	Kawasaki			JP
Horie; Takeshi	Kawasaki			JP
Shimizu; Toshiyuki	Kawasaki			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Fujitsu Limited	Kawasaki			JP	03
PFU Limited	Kahoku			JP	03

APPL-NO: 08/ 598243 [PALM]
DATE FILED: February 7, 1996

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	7-060500	March 20, 1995
JP	7-250527	September 28, 1995

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 711/141; 711/120, 711/147
US-CL-CURRENT: 711/141; 711/120, 711/147

FIELD-OF-SEARCH: 395/468, 395/471, 395/472, 395/447, 395/474, 395/475, 711/141, 711/144, 711/145, 711/120, 711/147, 711/148

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PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4136386	January 1979	Annunziata et al.	711/119
☐	4503497	March 1985	Krygowski et al.	711/124
☐	4622631	November 1986	Frank et al.	707/201
☐	5291442	March 1994	Emma et al.	711/120
☐	5522058	May 1996	Iwasa et al.	711/145
☐	5537569	July 1996	Masubuchi	711/121
☐	5568633	October 1996	Boudou et al.	711/141
☐	5606686	February 1997	Tarui et al.	711/121

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0049387	April 1982	EP	
0095598	December 1983	EP	
0301354-A2	February 1989	EP	
0397994-A2	November 1990	EP	
0489556	June 1992	EP	
0669578-A2	August 1995	EP	
60-215272	October 1985	JP	
62-282358	December 1987	JP	
4-305746	October 1992	JP	
6-110844	April 1994	JP	
7-6092	January 1995	JP	
WO 82/03480	October 1982	WO	
WO 90/00283	January 1990	WO	
WO-95/24678-A2	September 1995	WO	

ART-UNIT: 272

PRIMARY-EXAMINER: Swann; Tod R.

ASSISTANT-EXAMINER: King, Jr.; Conley B.

ATTY-AGENT-FIRM: Staas & Halsey

ABSTRACT:

A plurality of processors, each with caches provided for a plurality of processor

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modules and a local storage in which a main storage is distributed and arranged are mutually connected through an internal snoop bus. The processor modules are mutually connected through a second system bus. By using two separate buses, cache coherence operations within a processor group is kept separate from cache coherence operations outside the processor group.

60 Claims, 65 Drawing figures

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L1: Entry 2 of 37 File: USPT Jun 8, 2004

DOCUMENT-IDENTIFIER: US 6748465 B2
TITLE: Local bus polling support buffer

Detailed Description Text (23):
Maintaining a copy of data concerning I/O devices coupled to bus 250 in buffer 242 allows the number accesses that I/O controller 140 makes to memory 232 to be reduced. This reduction in accesses may, in turn, allow memory 232 to be powered down at times where memory 232 would otherwise have to be powered up to allow I/O controller 240 to make such accesses. In an embodiment of computer system 200 that is further comprised of cache 234, this reduction in accesses may also allow cache 234 to remain powered down along with memory 232 at times where cache 234 would otherwise have to be powered up to either respond to accesses being made by I/O controller 140, or to take steps necessary to maintain coherency between data stored in cache 234 and memory 232. In another embodiment of computer system 200 that is further comprised of cache 214, this reduction in accesses may also allow cache 214 to remain powered down, which may in turn, allow processor 210 to remain powered down at times where it would otherwise be necessary to be powered up in order to maintain coherency between data stored in cache 214 and memory 232. In still another embodiment of computer system 200, both caches 214 and 234 are present, either processor 210 or memory 232 and their associated caches may be powered down during the normal operation of computer system 200, as determined to be appropriate as part of whatever measures are being taken to reduce power consumption by computer system 200. In such an embodiment, the reduction in accesses to memory 232 would allow whichever ones of processor 210 or memory 232 and their associated caches to remain powered down.

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L1: Entry 2 of 37 File: USPT Jun 8, 2004

US-PAT-NO: 6748465
DOCUMENT-IDENTIFIER: US 6748465 B2

TITLE: Local bus polling support buffer

DATE-ISSUED: June 8, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Howard; John S.	Portland	OR		
Hosler; Brad	Portland	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 968073 [PALM]
DATE FILED: September 28, 2001

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/36; 710/46, 710/52, 711/147, 711/165, 713/320, 713/330
US-CL-CURRENT: 710/36; 710/46, 710/52, 711/147, 711/165, 713/320, 713/330

FIELD-OF-SEARCH: 710/1, 710/36, 710/46, 710/52, 711/147, 711/165, 713/320, 713/330

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4698748	October 1987	Juzswik et al.	713/322
☐	5293602	March 1994	Fukagawa et al.	711/147
☐	6141726	October 2000	Dell	711/103

ART-UNIT: 2182

PRIMARY-EXAMINER: Perveen; Rehana

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ATTY-AGENT-FIRM: Blakley, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

A method and apparatus for allowing memory, cache and/or a processor to remain powered down while repetitive transactions are carried out on an I/O bus and actions are taken in response to feedback received from I/O devices coupled to the I/O bus.

28 Claims, 3 Drawing figures

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L1: Entry 15 of 37 File: USPT Oct 16, 2001

DOCUMENT-IDENTIFIER: US 6304932 B1
TITLE: Queue-based predictive flow control mechanism with indirect determination of queue fullness

Detailed Description Text (30):
Finally, each module that has a cache memory, including both processor and input/output modules, has a cache coherency queue for storing coherent transactions in a first-in first-out ("FIFO") order. A coherent transaction is any transaction (such as a read) that results in the need to check other caches to see whether the requested data is in the other cache, or to verify that the cache is up-to-date. Such transactions are indicated by signals sent during the address cycle for the transactions initiated on bus 12. Each module having a cache memory monitors the bus and loads coherent transaction into its cache coherency queue, referred to herein as CCC queues. The coherent transactions wait in the CCC queue of a particular module until that module checks its cache, and reports the results of that coherency check to main memory controller 14. In a preferred implementation, main memory controller 14 begins reading the main memory as soon as the read transaction has been issued. Main memory controller 14 waits until the results of the coherency checks are reported by all of the modules, and then responds to the coherent transaction. If no client module has a private-dirty copy of the data, main memory controller 14 will supply the data from main memory. Otherwise, the client module that has a private-dirty copy will supply the data and main memory controller 14 will update main memory with the new data value. In a preferred implementation, coherency responses are received by main memory controller 14 quickly enough so that there is no appreciable delay in responding to the transaction.

L1: Entry 15 of 37 File: USPT Oct 16, 2001

US-PAT-NO: 6304932
DOCUMENT-IDENTIFIER: US 6304932 B1

TITLE: Queue-based predictive flow control mechanism with indirect determination of queue fullness

DATE-ISSUED: October 16, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ziegler; Michael L.	Whitinsville	MA		
Brooks; Robert J.	Roseville	CA		
Bryg; William R.	Saratoga	CA		
Frink; Craig R.	Chelmsford	MA		
Hotchkiss; Thomas R.	Groton	MA		
Odineal; Robert D.	Roseville	CA		
Williams; James B.	Lowell	MA		
Wood; John L.	Rochester	NH		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 09/ 697560 [PALM]
DATE FILED: October 25, 2000

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATION This is a continuation of application Ser. No. 08/201,185 filed on Feb. 24, 1994 now U.S. Pat. No. 6,182,176

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 710/112; 710/113
US-CL-CURRENT: 710/112; 710/113

FIELD-OF-SEARCH: 710/112, 710/113, 710/114, 710/115, 710/116, 710/117, 710/118

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

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☐	5265235	November 1993	Sindhu et al.	711/120

ART-UNIT: 273

PRIMARY-EXAMINER: Ellis; Richard L.

ABSTRACT:

A shared bus system having a bus and a set of client modules coupled to the bus. Each client module is capable of sending transactions on the bus to other client modules and receiving transactions on the bus from other client modules for processing. Each module has a queue for storing transactions received by the module for processing. A bus controller limits the types of transactions that can be sent on the bus to prevent any module's queue from overflowing.

3 Claims, 2 Drawing figures

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L1: Entry 17 of 37 File: USPT Jan 30, 2001

DOCUMENT-IDENTIFIER: US 6182176 B1
** See image for Certificate of Correction **
TITLE: Queue-based predictive flow control mechanism

Detailed Description Text (30):
Finally, each module that has a cache memory, including both processor and input/output modules, has a cache coherency queue for storing coherent transactions in a first-in first-out ("FIFO") order. A coherent transaction is any transaction (such as a read) that results in the need to check other caches to see whether the requested data is in the other cache, or to verify that the cache is up-to-date. Such transactions are indicated by signals sent during the address cycle for the transactions initiated on bus 12. Each module having a cache memory monitors the bus and loads coherent transaction into its cache coherency queue, referred to herein as CCC queues. The coherent transactions wait in the CCC queue of a particular module until that module checks its cache, and reports the results of that coherency check to main memory controller 14. In a preferred implementation, main memory controller 14 begins reading the main memory as soon as the read transaction has been issued. Main memory controller 14 waits until the results of the coherency checks are reported by all of the modules, and then responds to the coherent transaction. If no client module has a private-dirty copy of the data, main memory controller 14 will supply the data from main memory. Otherwise, the client module that has a private-dirty copy will supply the data and main memory controller 14 will update main memory with the new data value. In a preferred implementation, coherency responses are received by main memory controller 14 quickly enough so that there is no appreciable delay in responding to the transaction.

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L1: Entry 17 of 37 File: USPT Jan 30, 2001

US-PAT-NO: 6182176
DOCUMENT-IDENTIFIER: US 6182176 B1
**** See image for Certificate of Correction ****

TITLE: Queue-based predictive flow control mechanism

DATE-ISSUED: January 30, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ziegler; Michael L.	Whitinsville	MA		
Brooks; Robert J.	Roseville	CA		
Bryg; William R.	Saratoga	CA		
Frink; Craig R.	Chelmsford	MA		
Hotchkiss; Thomas R.	Groton	MA		
Odineal; Robert D.	Roseville	CA		
Williams; James B.	Lowell	MA		
Wood; John L.	Rochester	NH		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 08/ 201185 [PALM]
DATE FILED: February 24, 1994

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 710/112; 710/113
US-CL-CURRENT: 710/112; 710/113

FIELD-OF-SEARCH: 395/250, 395/400, 395/425, 395/325

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5204954	April 1993	Hammer et al.	395/425
☐	5257374	October 1993	Hammer et al.	395/650

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☐	5265235	November 1993	Sindhu et al.	395/425

OTHER PUBLICATIONS

U.S. application No. 0497054A3, Sindhu et al., filed Aug. 5, 1992.
U.S. application No. 0317468A3, Hammer et al., filed May 24, 1989.

ART-UNIT: 273

PRIMARY-EXAMINER: Ellis; Richard L.

ABSTRACT:

A shared bus system having a bus and a set of client modules coupled to the bus. Each client module is capable of sending transactions on the bus to other client modules and receiving transactions on the bus from other client modules for processing. Each module has a queue for storing transactions received by the module for processing. A bus controller limits the types of transactions that can be sent on the bus to prevent any module's queue from overflowing.

1 Claims, 2 Drawing figures

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L1: Entry 35 of 37 File: USPT May 12, 1992

DOCUMENT-IDENTIFIER: US 5113514 A
TITLE: System bus for multiprocessor computer system

Abstract Text (1):
The invention comprises a system bus apparatus and method for a multi-arm, multiprocessor computer system having a main memory and localized buffer cache memories at each processor. Each block of data in a cache includes tag bits which identifies the condition of the data block in relation to the corresponding data in main memory and other caches. The system bus (SYSBUS) comprises three subparts; 1) a MESSAGE/DATA bus, 2) a REQUEST/GRANT bus and 3) a BCU bus. The MESSAGE/DATA bus is coupled to every device on the system and is used for transferring messages, data and addresses. The REQUEST/GRANT bus couples between every device on an arm of the system and that arm's bus control unit (BCU). The BCU bus couples between the various BCUs. Both the MESSAGE/DATA bus and the BCU bus include ACK/NACK/HIT bits which are used when responding to messages received over the SYSBUS to inform the message-issuing device if the devices received the message and, if so, the condition of the data in relation to other caches and main memory. The protocol allows inconsistent copies of data to exist and prevents stale data from being used erroneously by monitoring the tag bits and the ACK/NACK/HIT bits. Further, under the appropriate conditions, a copy of the most recent data block may be transferred from one cache to another (with appropriate updating of tags) without updating the main memory. When a memory operation will bring about a situation where cache coherence can no longer be maintained, main memory is updated with the most recent copy of the data and the other caches are either updated or tagged as invalid.

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L1: Entry 35 of 37 File: USPT May 12, 1992

US-PAT-NO: 5113514
DOCUMENT-IDENTIFIER: US 5113514 A

TITLE: System bus for multiprocessor computer system

DATE-ISSUED: May 12, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Albonesi; David H.	Hudson	MA		
Langendorf; Brian K.	Shrewsbury	MA		
Chang; John	Morton Grove	IL		
Faase; John G.	Palo Alto	CA		
Homberg; Michael J.	Grafton	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Prime Computer, Inc.	Framingham	MA			02

APPL-NO: 07/ 482288 [PALM]
DATE FILED: February 20, 1990

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATION This application is a continuation of application Ser. No. 07/397,124, filed Aug. 22, 1989 now abandoned.

INT-CL: [05] G06F 12/00, G06F 13/00

US-CL-ISSUED: 395/425
US-CL-CURRENT: 711/144; 711/145

FIELD-OF-SEARCH: 365/49

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4785394	November 1988	Fischer	364/200
☐	4785395	November 1988	Keeley	364/200
☐	4928225	May 1990	McCarthy et al.	364/200

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J. Archibald & J. Baer, Cache Coherence Protocols: Evaluation Using A Multiprocessor Simulation Model, ACM Transactions on Computer Systems, vol. 4, No. 4 (Nov. 1986).

ART-UNIT: 232

PRIMARY-EXAMINER: Bowler; Alyssa H.

ATTY-AGENT-FIRM: Wolf, Greenfield & Sacks

ABSTRACT:

The invention comprises a system bus apparatus and method for a multi-arm, multiprocessor computer system having a main memory and localized buffer cache memories at each processor. Each block of data in a cache includes tag bits which identifies the condition of the data block in relation to the corresponding data in main memory and other caches. The system bus (SYSBUS) comprises three subparts; 1) a MESSAGE/DATA bus, 2) a REQUEST/GRANT bus and 3) a BCU bus. The MESSAGE/DATA bus is coupled to every device on the system and is used for transferring messages, data and addresses. The REQUEST/GRANT bus couples between every device on an arm of the system and that arm's bus control unit (BCU). The BCU bus couples between the various BCUs. Both the MESSAGE/DATA bus and the BCU bus include ACK/NACK/HIT bits which are used when responding to messages received over the SYSBUS to inform the message-issuing device if the devices received the message and, if so, the condition of the data in relation to other caches and main memory. The protocol allows inconsistent copies of data to exist and prevents stale data from being used erroneously by monitoring the tag bits and the ACK/NACK/HIT bits. Further, under the appropriate conditions, a copy of the most recent data block may be transferred from one cache to another (with appropriate updating of tags) without updating the main memory. When a memory operation will bring about a situation where cache coherence can no longer be maintained, main memory is updated with the most recent copy of the data and the other caches are either updated or tagged as invalid.

28 Claims, 19 Drawing figures

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US-PAT-NO: 6122659

DOCUMENT-IDENTIFIER: US 6122659 A

TITLE: Memory controller for controlling memory accesses across networks in distributed shared memory processing systems

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Brief Summary Text - BSTX (27):

A cache coherency system for a shared memory parallel processing system including plurality of processing nodes. A multi-stage communication network is provided for interconnecting the processing nodes. Each processing node includes one or more caches for storing a plurality of cache lines. A cache coherency directory is distributed to each of the nodes for tracking which of the nodes have copies of each cache line. A plurality of send FIFOs and receive FIFOs are used at each node adapter to segregate and handle invalidate functions, remote stores, and remote reads requiring cache coherency.

US006122659A

United States Patent [19]

Olnowich

[11] Patent Number: 6,122,659

[45] Date of Patent: Sep. 19, 2000

[54] **MEMORY CONTROLLER FOR CONTROLLING MEMORY ACCESSES ACROSS NETWORKS IN DISTRIBUTED SHARED MEMORY PROCESSING SYSTEMS**

[75] Inventor: **Howard Thomas Olnowich**, Endwell, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **09/394,565**

[22] Filed: **Sep. 10, 1999**

Related U.S. Application Data

[62] Division of application No. 08/890,341, Jul. 10, 1997, Pat. No. 6,044,438.

[51] **Int. Cl.**[7] **G06F 15/167; G06F 12/00**

[52] **U.S. Cl.** **709/213**; 709/214; 711/120; 707/201

[58] **Field of Search** 709/213, 214; 711/120, 130, 142, 150; 707/201

[56] **References Cited**

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M. Dubois et al. "Effects of Cache Coherency in Multiprocessors", *IEEE Transactions on Computers*, vol. C-31, No. 11, Nov. 1982.

Primary Examiner—Krisna Lim

Attorney, Agent, or Firm—Shelley M Beckstrand

[57] **ABSTRACT**

A shared memory parallel processing system interconnected by a multi-stage network combines new system configuration techniques with special-purpose hardware to provide remote memory accesses across the network, while controlling cache coherency efficiently across the network. The system configuration techniques include a systematic method for partitioning and controlling the memory in relation to local verses remote accesses and changeable verses unchangeable data. Most of the special-purpose hardware is implemented in the memory controller and network adapter, which implements three send FIFOs and three receive FIFOs at each node to segregate and handle efficiently invalidate functions, remote stores, and remote accesses requiring cache coherency. The segregation of these three functions into different send and receive FIFOs greatly facilitates the cache coherency function over the network. In addition, the network itself is tailored to provide the best efficiency for remote accesses.

24 Claims, 41 Drawing Sheets